FIG. 1

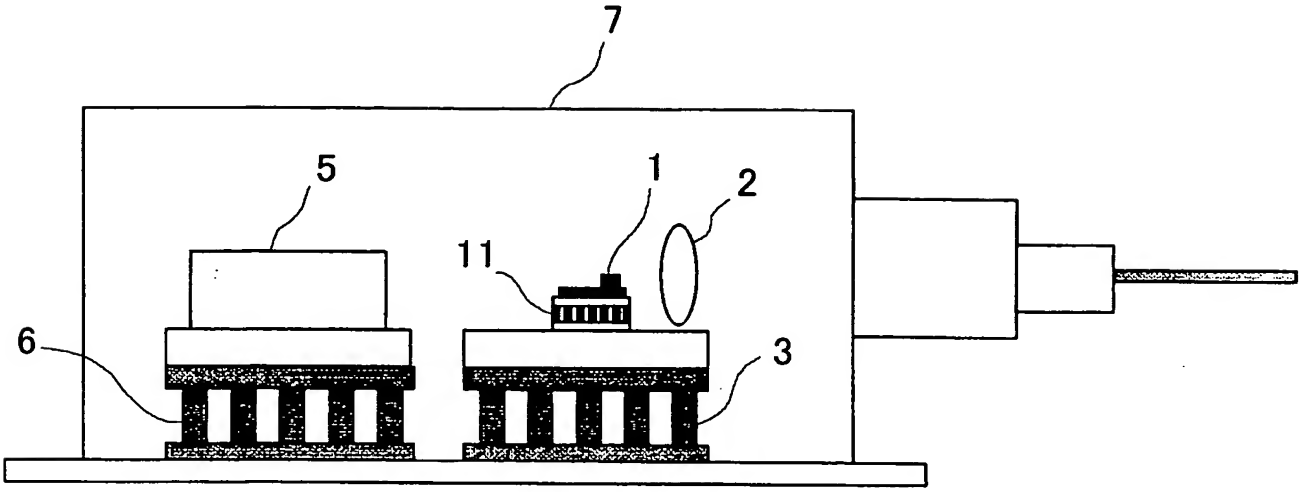


FIG. 2

| LD Heating value Q mW | Peltier substrate area S ($mm^2$) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 2 | 4 | 8 | 16 | 32 | 64 |
| 150 | 75 | 37.5 | 18.75 | 9.375 | 4.6875 | 2.34375 |
| 250 | 125 | 62.5 | 31.25 | 15.625 | 7.8125 | 3.90625 |
| 360 | 180 | 90 | 45 | 22.5 | 11.25 | 5.625 |
| 600 | 300 | 150 | 75 | 37.5 | 18.75 | 9.375 |
| 800 | 400 | 200 | 100 | 50 | 25 | 12.5 |
| 1000 | 500 | 250 | 125 | 62.5 | 31.25 | 15.625 |

FIG. 3A

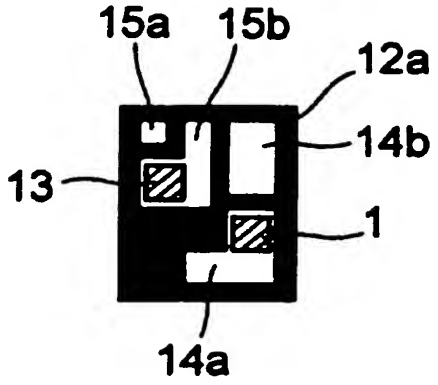



FIG. 3B

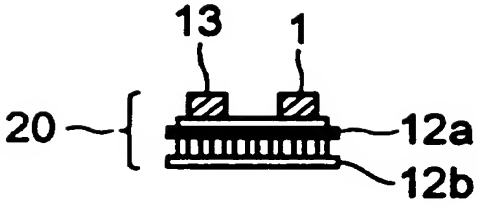
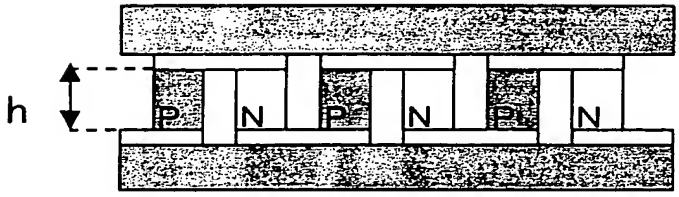



FIG. 3C



# FIG. 4

| | Symbol | Unit | Example | | | | | | Comparative Example | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Config.A | Config.B | Config.C | Config.D | Config.E | Config.F | Config.G | Config.H | Config.I | Config.J |
| ■ Ratio of element heating value to first substrate area | Qd/S1 | mW/mm^2 | 55.56 | 55.56 | 32.61 | 160.00 | 55.56 | 52.08 | 7.50 | 20.00 | 7.03 | 20.83 |
| ■ Area ratio of first substrate to second subsutrate | S1/S2 | | 0.090 | 0.090 | 0.219 | 0.031 | 0.045 | 0.120 | 1.000 | 0.625 | 1.000 | 0.750 |
| ■ Mode coefficient of TEC | F | mm | 9.07 | 9.52 | 24.30 | 9.22 | 4.54 | 12.10 | 25.79 | 29.65 | 36.11 | 49.41 |
| ■ Area of first substrate | S1 | mm^2 | 6.48 | 6.48 | 18.40 | 2.25 | 3.24 | 8.64 | 48.00 | 30.00 | 64.00 | 48.00 |
| ■ Sum of chip bottom area | Sc1 | mm^2 | 1.81 | 4.76 | 8.51 | 0.92 | 0.91 | 2.42 | 19.60 | 15.12 | 27.44 | 25.20 |
| ■ Element heating value | Qd | mW | 360 | 360 | 600 | 360 | 180 | 450 | 360 | 600 | 450 | 1000 |
| ■ Ratio of element heating value to sum of chip bottom area | Qd/Sc | mW/mm^2 | 198.41 | 75.66 | 70.55 | 390.63 | 198.41 | 186.01 | 18.37 | 39.68 | 16.40 | 39.68 |
| ■ Power consumption (ambient temperature of 70°C/LD temperature of 0°C) | W | W | 2.50 | 2.50 | 4.00 | 2.10 | 2.00 | 3.50 | 5.00 | 5.50 | 5.50 | 9.00 |

FIG. 5

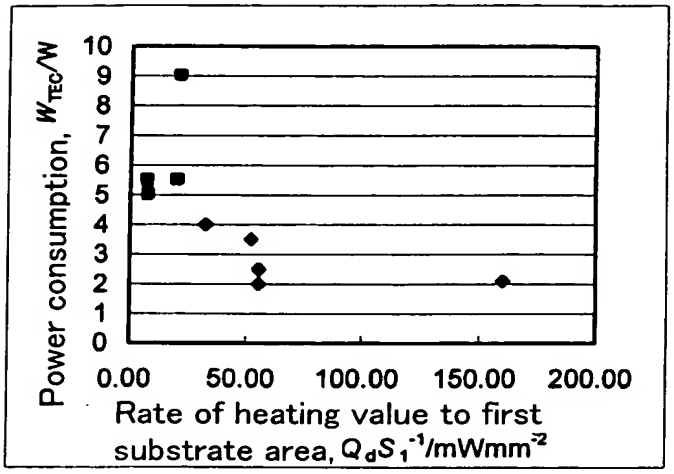

Power consumption, $W_{TEC}$/W
10
9
8
7
6
5
4
3
2
1
0
0.00
50.00
100.00
150.00
200.00
Rate of heating value to first substrate area, $Q_d S_1^{-1}$/mWmm$^{-2}$

FIG. 6

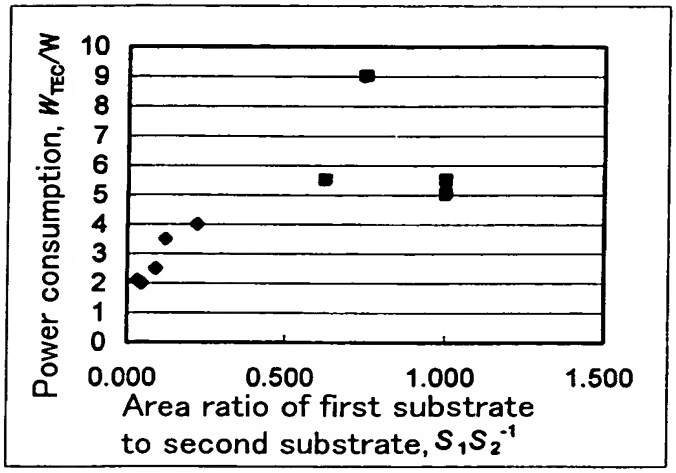

Power consumption, $W_{TEC}$/W
10
9
8
7
6
5
4
3
2
1
0
0.000
0.500
1.000
1.500
Area ratio of first substrate to second substrate, $S_1 S_2^{-1}$

FIG. 7

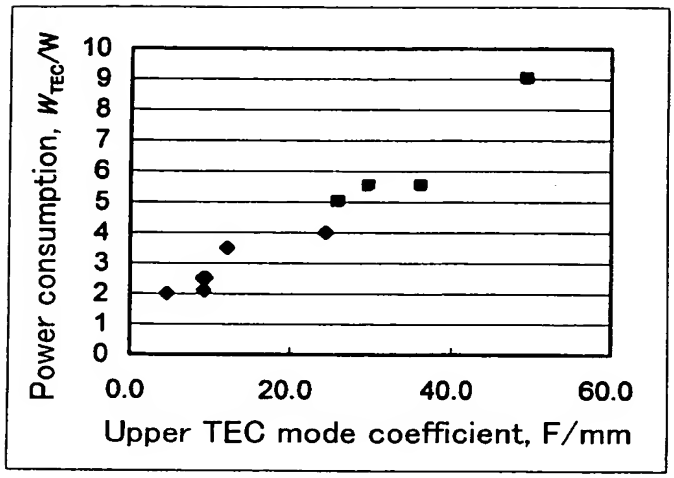

Power consumption, $W_{TEC}$/W
10
9
8
7
6
5
4
3
2
1
0
0.0
20.0
40.0
60.0
Upper TEC mode coefficient, F/mm

FIG. 8

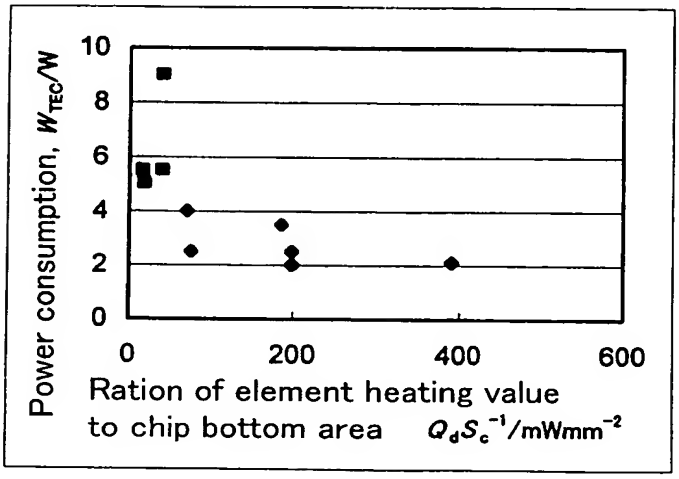

Power consumption, $W_{TEC}$/W
10
8
6
4
2
0
0
200
400
600
Ration of element heating value
to chip bottom area $Q_d S_c^{-1}$/mWmm$^{-2}$

FIG. 9

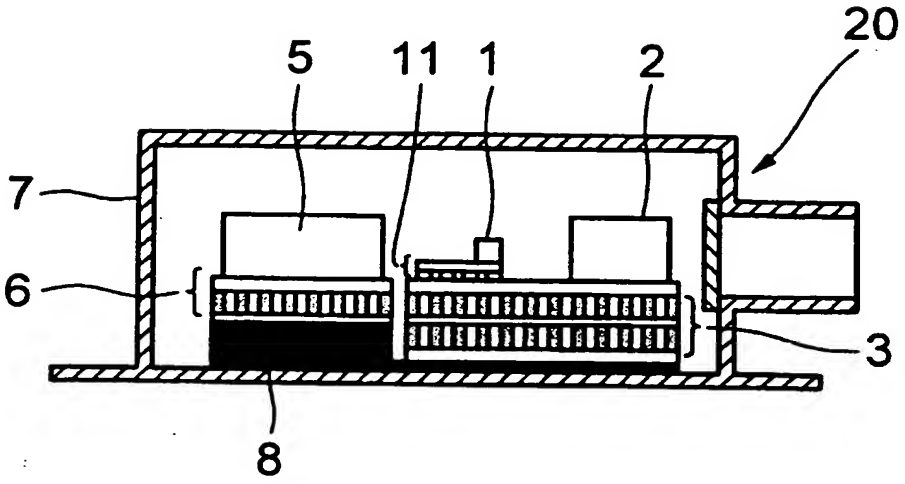



FIG. 10

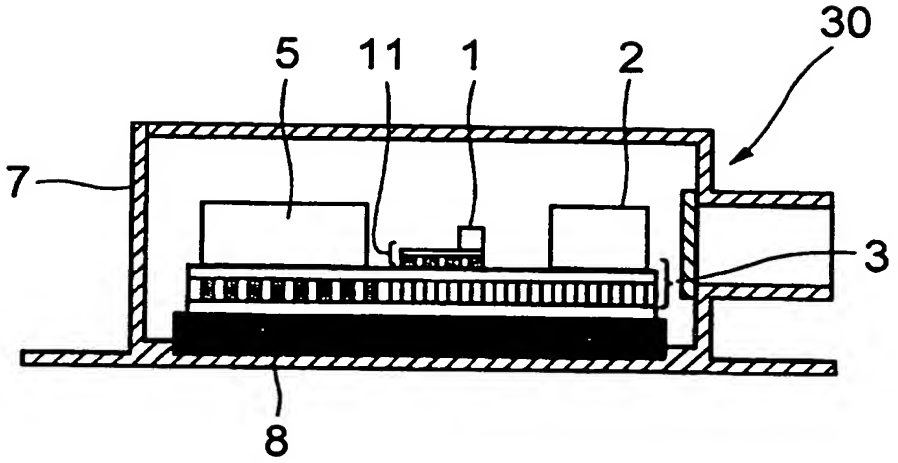


FIG. 11